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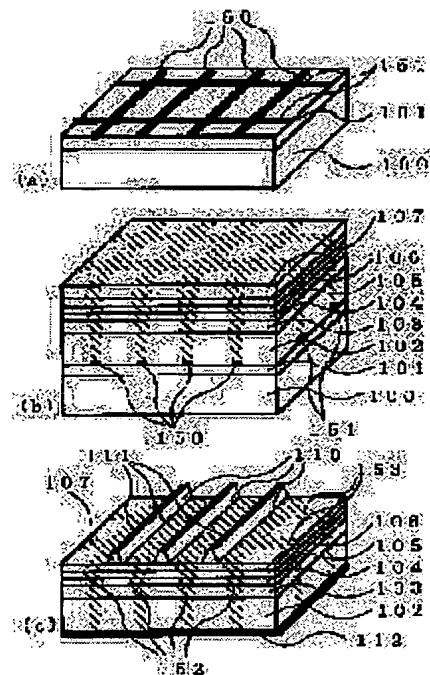
(72)Inventor : TANETANI MOTOTAKA

(54) SEMICONDUCTOR LIGHT EMITTING DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent the decline in the light emission efficiency by forming a light emitting region generated by current injection which is one of active layers, in other region than a region right above a growth suppressing structure.

SOLUTION: On a sapphire substrate 100, selectively grown masks 150, 151 are so formed as to cross at right angles each other. After that, an n-GaN continuous film semiconductor layer 102 is grown. Then, a mesa stripe 110 is formed nearly parallelly with the selectively grown mask 150 in other region than a region 152 right above the selectively grown mask 150. Next, a p-type electrode 111 of a stripe geometry is formed on an upper face of the mesa stripe 110 and then a backside of a wafer is polished to expose the n-GaN continuous film semiconductor layer 102 and an n-type electrode 112 is formed on the entire surface of the n-GaN continuous film semiconductor layer 102. After that, at a position away from the selectively grown mask 151, a mirror surface which constitutes a laser resonator is formed by cleaving. By specifying the shape of the selectively grown masks, the relative position of the mesa stripe 110, and the relative position of the laser resonator mirror for cleaving, the decline in the light emission efficiency can be prevented.



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(71) 出願人 000005049

シャープ株式会社

大阪府大阪市阿倍野区長池町22番22号

(72) 発明者 種谷 元隆

大阪府大阪市阿倍野区長池町22番22号

シャープ株式会社内

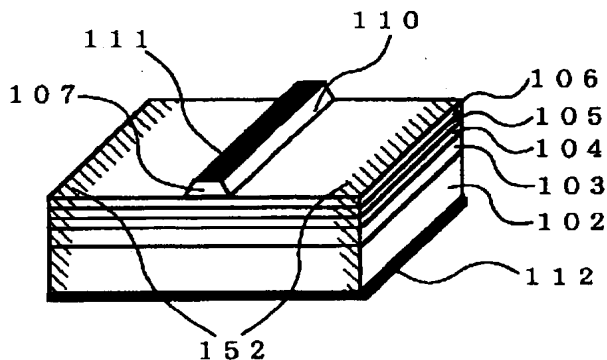
(74) 代理人 弁理士 小池 隆彌

(54) 【発明の名称】 半導体発光素子及びその製造方法

(57) 【要約】

【課題】 部分的成長抑制構造を利用して、基板と格子定数または熱膨張係数が異なる連続膜半導体層を形成した上に、さらに半導体発光素子を形成する場合の発光効率の低下および信頼性の悪化を防止する。

【解決手段】 成長抑制構造上への結晶成長により得られる成長抑制構造上方領域を含む連続膜半導体層の上に形成された半導体発光素子において、活性層の内、電流注入により光を発生する発光領域が上記成長抑制構造上方領域以外の領域に形成されているようにする。



【特許請求の範囲】

【請求項1】 成長抑制構造上への結晶成長により得られる成長抑制構造直上領域を含む連続膜半導体層と、光を発生させる活性層とを有する半導体発光素子であって、

該活性層の内、電流注入により光を発生する発光領域が前記成長抑制構造直上領域以外の領域に形成されていることを特徴とする半導体発光素子。

【請求項2】 前記発光領域は成長抑制構造直上領域から30 μ m以上離れた位置に形成されていることを特徴とする請求項1に記載の半導体発光素子。

【請求項3】 前記発光領域と前記成長抑制構造直上領域との間の領域では、前記活性層が除去されていることを特徴とする半導体発光素子。

【請求項4】 基板上に成長抑制構造を形成する第1工程と、

前記基板および前記成長抑制構造の両方を連続して覆うように前記基板と格子定数または熱膨張係数が異なる連続膜半導体層を形成する第2工程と、

前記連続膜半導体層の上に光を発生させる活性層を含む多層構造体を形成する第3工程と、

前記成長抑制構造部の直上領域を除いて前記活性層における発光領域を規定するための構造を形成する第4工程と、を有することを特徴とする半導体発光素子の製造方法。

【請求項5】 半導体発光素子をウェハから複数の半導体発光素子に分割する工程を有する半導体発光素子の製造方法であって、

前記第4工程後、前記成長抑制構造直上の前記活性層が半導体発光素子に含まれないように半導体発光素子をウェハから分割する第5工程とを含むことを特徴とする請求項4に記載の半導体発光素子の製造方法。

【請求項6】 前記第5工程において、前記成長抑制構造直上の端から30 μ m以内の領域に残存する前記活性層が、半導体発光素子に含まれないように半導体発光素子を分割することを特徴とする請求項5に記載の半導体発光素子の製造方法。

【発明の詳細な説明】**【0001】**

【発明の属する技術分野】 本発明は、半導体発光素子に関し、特に、基板上に基板とは格子定数または熱膨張係数の異なる半導体材料にて形成された信頼性の高い半導体発光素子に関する。

【0002】

【従来の技術】 半導体発光素子を構成する結晶材料とは格子定数が3%以上異なる基板上へ形成する場合や、熱膨張係数が10%以上異なる基板上へ半導体結晶を成長する場合には、まず基板の上に半導体発光素子を構成する材料と格子定数や熱膨張係数がほぼ等しい（格子定数、熱膨張係数とも1%以内）結晶材料を厚く成長させ

連続膜半導体層を形成した上に半導体発光素子を形成する試みがなされている。連続膜半導体層の上に積層した半導体層は結晶欠陥が低減することが報告されている。このような発光素子の代表例として、図8に、サファイア基板800上に、Ga_{0.9}N層を厚く結晶成長させて連続膜半導体層を形成し、その上に青色発光ダイオード（LED）を形成した従来技術による例を示す。

【0003】 この従来例のLEDの作製方法を説明する。サファイア基板800上に、まずハライド気相成長法（HVPE法）によりGa_{0.9}N層801を5 μ m厚に厚く成長させる。次に、Ga_{0.9}N層801表面にSiO₂からなる選択成長マスク802を格子状（200 μ mピッチの20 μ m幅のSiO₂ストライプが互いに直交する形）に形成する。以上までに作製された工程断面図を図8（a）に示す。

【0004】 次に、このサファイア基板800上にHVPE法によりn型Ga_{0.9}N連続膜半導体層803を300 μ m厚成長させる。この時、HVPE工程により成長されたn型Ga_{0.9}N連続膜半導体層803は、サファイア基板800が露出した部分から成長が始まるが、その厚さが増すに伴い、SiO₂からなる選択成長用マスク802上へ張り出すように左右へも成長し、最終的には20 μ m幅のSiO₂からなる選択成長マスク802上を覆った。このようにして、表面が平坦なn型Ga_{0.9}N連続膜半導体層803が形成された。

【0005】 次に、このサファイア基板800上にn型Ga_{0.9}N連続膜半導体層803が形成されたウェハに、有機金属気相成長法（MOCVD法）によりn-GaNクラッド層804、InGa_{0.9}N活性層805、p-GaNコンタクト層806が形成された。以上までに作製された工程断面図を図8（b）に示す。

【0006】 次に、図9の（a）従来例のLEDの上面構造図と（b）従来例LEDのA-A'断面図に示すように、300 μ m角の発光領域810を残し、その回りを取り囲むように通常のフォトリソグラフィ技術とドライエッチング技術を用いてp-GaNコンタクト層806、InGa_{0.9}N活性層805、n-GaNクラッド層804を貫通するように除去し、n型Ga_{0.9}N連続膜半導体層803を露出させた。最後に、n型Ga_{0.9}N連続膜半導体層803の表面にn型電極807を、300 μ m角のp-GaNコンタクト層806の表面に光透過性を有するp型電極808をそれぞれ形成した。このようにして、作製したウェハから、発光領域810の周辺でスクライプし、個々のLEDを切り出し素子とした。このようにして作製する従来例のLEDが報告されている。

【0007】

【発明が解決しようとする課題】 しかしながら、このようにして作製したLEDの特性を当該発明者が試験した結果、20mAの電流を注入した場合の発光効率（電子の光子への変換効率）が個々の素子により0.3%から

10%と大きく異なり、所望の5%以上の発光効率が得られる歩留まりが2%と非常に低いことや、80℃の条件下での約100時間の初期信頼性試験にて全ての素子の発光効率が試験開始時の約30%以下に激減することが新たに判明した。

【0008】これらの従来素子の不良について、当該発明者が詳細な検討を行った結果、下記のような事実が判明した。

(1) 選択成長マスク802の存在する選択成長マスク直上領域811に位置するInGaN活性層805部分での発光が非常に小さい。また、この発光効率の低下はチップの発光領域810の周辺領域より発光領域810の中央領域に選択成長マスク直上領域811が位置する場合に特に顕著になることも分かった。これにより、選択成長マスク直上領域811が発光領域810のどの部分に位置しているかにより、大きく発光効率が変化する。

(2) 上記の信頼性不良の素子においても、100時間の信頼性試験走行後では、選択成長マスク直上領域811(幅20 μ m)のInGaN活性層805はその近傍の両側約30 μ mを含め、合計80 μ mの領域で発光がほとんど認められない。

【0009】さらに従来例素子の結晶解析を行った結果、選択成長マスク直上領域811に位置するInGaN活性層805には、厚さ300 μ mのn型Ga_{0.5}N連続膜半導体層803を貫通して結晶転移が集中して導入されていることが明確になった。図10にInGaN活性層805における結晶転移の密度を、選択成長マスク802端からの距離をパラメータとして測定した結果を示す。幅20 μ mの選択成長マスク直上領域811のInGaN活性層805には密度 10^{12} cm⁻²の結晶転移が集中しており、さらに選択成長マスク802の端から10 μ m離れた位置でも 10^{11} cm⁻²の転移が観測された。選択成長マスク802の端から離れるにつれて結晶転移は減少し、30 μ m以上離れた場所のInGaN活性層805では結晶転移は $10^7 \sim 10^8$ cm⁻³にまで減少した。このような傾向は、上記のように作製されたウェハのいずれの部分でも観測された。

【0010】また、同様な方法により半導体レーザを上述のようなn型Ga_{0.5}N連続膜半導体層803上に、発光領域に選択成長マスク直上領域811が含まれ、発振閾値電流が700mAと大きく、かつ素子寿命も室温において1秒程度と非常に短かった。

【0011】上記のように、従来技術においては、下記のような問題点が明らかになった。

(1) 選択成長法を用いて作製した連続膜半導体層上の発光素子において、選択成長マスク直上領域811において発光効率の低下が見られるため、発光領域に選択成長マスク直上領域が含まれるチップでは劇的に発光効率が低下する。

(2) GaN連続膜の上に形成した半導体レーザ素子の寿命が短く、半導体レーザ素子は得られなかった。

【0012】このため、基板上に、基板と異なる格子定数や熱膨張係数を有する連続膜半導体層を成長させ、その上に形成する半導体発光素子に、格子定数差や熱膨張係数差から引き起こされる発光効率の低下や信頼性不良を防止することは不可能であった。

【0013】従って、部分的成長抑制構造を利用して、基板と格子定数または熱膨張係数が異なる連続膜半導体層を形成した上に、さらに半導体発光素子を形成する場合における発光効率の低下および信頼性の悪化を防止することを目的とする。

【0014】

【課題を解決するための手段】本発明の請求項1は、成長抑制構造上への結晶成長により得られる成長抑制構造直上領域を含む連続膜半導体層と、光を発生させる活性層とを有する半導体発光素子であって、該活性層の内、電流注入により光を発生する発光領域が前記成長抑制構造直上領域以外の領域に形成されていることにより構成されている。

【0015】本発明における請求項2は、前記発光領域は成長抑制構造直上領域から30 μ m以上離れた位置に形成されていることにより構成され、さらに請求項3は前記発光領域と前記成長抑制構造直上領域との間の領域では、前記活性層が除去されていることにより構成されている。

【0016】一方、請求項4は、基板上に成長抑制構造を形成する第1工程と、前記基板および前記成長抑制構造の両方を連続して覆うように前記基板と格子定数または熱膨張係数が異なる連続膜半導体層を形成する第2工程と、前記連続膜半導体層の上に光を発生させる活性層を含む多層構造体を形成する第3工程と、前記成長抑制構造部の直上領域を除いて前記活性層における発光領域を規定するための構造を形成する第4工程と、を有することにより構成されており、さらに請求項5は、半導体発光素子をウェハから複数個の半導体発光素子に分割する工程を有する半導体発光素子の製造方法であって、前記第4工程後、前記成長抑制構造直上の前記活性層が半導体発光素子に含まれないように半導体発光素子をウェハから分割する第5工程とを含むことにより構成され、請求項6は、前記第5工程において、前記成長抑制構造直上の端から30 μ m以内の領域に残存する前記活性層が、半導体発光素子に含まれないように半導体発光素子を分割することにより構成されている。

【0017】

【発明の実施の形態】以下に本発明を実施した例を用いて説明する。

(実施の形態1) 図1に本発明を実施した半導体レーザ素子の一例を示す。本半導体レーザ素子は、n-GaN連続膜半導体層102、n-GaNバッファ層103、

n-Al_{0.1}Ga_{0.9}Nクラッド層104、多重量子井戸活性層105、p-Al_{0.1}Ga_{0.9}Nクラッド層106、p-GaNコンタクト層107から構成されており、リッジ導波路としてレーザの発光領域を規定するためのメサストライプ110、さらには、電流注入用のp型電極111、n型電極112から構成されている。

【0018】次に、図2を用いて本実施例素子の作製工程を説明する。まず、サファイア基板100の上にMOCVD法によりGaNバッファ層101を1μm厚成長させる。次に、GaNバッファ層101の表面上に通常のスパッタ法によりSiO₂膜を0.4μm厚形成させた後、通常のフォトリソグラフィ技術とエッチング技術により幅10μmでピッチ150μmの周期的SiO₂からなる選択成長マスク150と幅10μmでピッチ500μmの周期的SiO₂からなる選択成長マスク151とが互いに直交する形状に形成した。以上までに作製された半導体レーザ素子の工程断面図を図2(a)に示す。

【0019】続いて、このウェハ上にHVPE法により、n-GaN連続膜半導体層102を150μm厚成長させた。基板温度は1020℃として35分の成長により150μm厚の成長が完了した。この成長時、選択成長マスク150、151が成長抑制構造として働くため、従来例にて説明のように、成長初期にはGaNバッファ層101が露出した領域でのみ成長は起こり、次第に、選択成長マスク150、151上に横方向に成長が進み、最終的に150μm厚の成長が終了した段階では、n-GaN連続膜半導体層102は連続膜を呈しており、その表面はスムーズになった。

【0020】次に、引き続きMOCVD法により、このn-GaN連続膜半導体層102の上に、n-GaNバッファ層103を0.5μm厚、n-Al_{0.1}Ga_{0.9}Nクラッド層104を0.2μm厚、4nm厚のIn_{0.25}Ga_{0.75}N井戸層2層と3nm厚のIn_{0.05}Ga_{0.95}Nバリア層3層からなる多重量子井戸活性層105、p-Al_{0.1}Ga_{0.9}Nクラッド層106を0.2μm厚、p-GaNコンタクト層107を0.7μm厚成長させた。以上までに作製された半導体レーザ素子の工程断面図を図2(b)に示す。

【0021】続いて、幅2μm、高さ0.7μmのメサストライプ110を選択成長マスク150の直上領域152以外の領域に選択成長マスク150とほぼ平行に形成した。この時、メサストライプ110が素子の上方から観察して隣り合う選択成長マスク150のほぼ中央に位置するようにした。このメサストライプ110の形成には通常のフォトリソグラフィ技術とドライエッチング技術を適用した。この後、メサストライプ110を上面にストライプ状のp型電極111を形成した後、ウェハ裏面を研磨することによりウェハ厚さを約120μmとし(すなわち、サファイア基板100、GaNバッ

ファ層101、選択成長マスク150、151を完全に除去し、n-GaN連続膜半導体層102がウェハ裏面に露出するようにし)、n-GaN連続膜半導体層102の露出した裏面の全面にn型電極112を形成した。以上までに作製された半導体レーザ素子の工程断面図を図2(c)に示す。

【0022】次に、劈開によりレーザ共振器を構成するミラー面を形成した。この劈開工程は以下のようにして実施した。まず、ウェハ裏面(すなわちn-GaN連続膜層103側)の隅近傍の2箇所にけがき傷を入れ、このけがき傷の位置において、選択成長マスク151を形成した方向と平行方向に劈開してレーザ共振器ミラーを形成した。この時、2箇所のけがき傷は互いに隣接する選択成長マスク151のエッジ部分から50μm離れた位置に形成し、選択成長マスク151の直上領域153がレーザ素子に含まれないようにした。従って、レーザ共振器長は400μmであった。最後に、選択成長マスク150の直上領域152の部分をスクライブし、個々のレーザチップに分割した。以上の工程を経て図1に示すレーザ素子が完成する。

【0023】以上のようにして作製したレーザ素子は、閾値電流25mAでレーザ発振が実現できた。また、本レーザ素子を50℃雰囲気、3mW出力の条件下において信頼性試験を実施した結果、初期の50時間以内に故障に至るレーザ素子を除いて、ほとんどの素子において1000時間以上の寿命が確認でき、メディアン寿命(試験した半分の素子が故障する時間)は1500時間であった。この信頼性は当該素子を光ディスク用光源として利用する場合にでも十分な特性である。この信頼性の改善は、本レーザ素子では、n-GaN連続膜半導体層102を成長させるために形成した成長抑制構造である選択成長マスク150、151上において結晶欠陥が集中する直上領域152、153がレーザ素子の発光領域(この場合は活性層105に電流が選択的に注入されるメサストライプ110が形成されている部分)に含まれないように、選択成長マスク150、151の形状と、選択成長マスク150に対するメサストライプ110の相対位置、および選択成長マスク151に対するレーザ共振器ミラーの劈開のための相対位置を設定したことによるものと理解できる。

【0024】上記の発明を実施したレーザ素子では、メサストライプ110を隣接する選択成長マスク150の直上領域152同士の間中央となるように(すなわち、選択成長マスク150の端から70μm離れた部分に)形成されている。上記の実施例素子と同様の構造で、メサストライプ110の直上領域152(すなわち選択成長マスク150)の端からの距離を0μm(すなわち直上領域152内にメサストライプ110を形成した場合)、10μm、20μm、30μm、50μm、70μmと変化させたレーザ素子を作製し、上記と同様の信頼性試

験を実施した。この時、素子分離ためのスクライブ位置はいずれの素子においても隣接するメサストライプ110の中心付近とし、スクライブ位置のメサストライプ110との相対距離を一定とした。その結果を図3に示す。横軸は直上領域152の中心からメサストライプ110までの距離、縦軸はメディアン寿命を示している。この結果から、実用上必要とされる1000時間以上のメディアン寿命を確保するためにはメサストライプ110を直上領域152から30 μ m以上離れた位置に形成することが必要であることが分かった。

【0025】(実施の形態2)次に、本発明を発光ダイオードに適用した場合について述べる。図4に第2の実施形態素子の構造図を示す。n-GaN連続膜半導体層401、n-GaNバッファ層402、 $\text{In}_{0.1}\text{Ga}_{0.9}\text{N}$ 歪み緩和層403、 $\text{In}_{0.5}\text{Ga}_{0.5}\text{N}$ 単一量子井戸活性層404、p- $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ 蒸発防止層405、p-GaNコンタクト層406、およびn型電極407、p型電極408から構成されている。また本実施例の素子ではメサ410により発光領域が規定されている。

【0026】次に、本発光素子の作製方法について説明する。まず、サファイア基板400表面にダイシングにより幅40 μ m、深さ50 μ mの溝構造450を400 μ mピッチで格子状に形成する。以上までに作製された半導体素子の工程断面図を図5(a)に示す。

【0027】次にHVPE法により、厚さ300 μ mのn-GaN連続膜半導体層401を成長させる。この時、サファイア基板400に形成した溝構造450があるため成長初期においてn-GaN連続膜半導体層401は平坦な面としての成長ができないが、成長厚を増すに従って徐々に左右の壁からの成長により溝構造450を埋まり、表面の溝は平坦に埋め込まれることとなった。すなわち、実効的に溝450での成長が遅いと同様の効果を実現でき、300 μ mの成長終了時にはn-GaN連続膜層401は、連続した表面が平坦な単一の層にすることができた。

【0028】次に、分子線エピタキシャル法(MBE法)により、n-GaN連続膜半導体層401上にn-GaNバッファ層402を0.4 μ m厚、 $\text{In}_{0.2}\text{Ga}_{0.8}\text{N}$ 歪み緩和層403を0.05 μ m厚、 $\text{In}_{0.45}\text{Ga}_{0.55}\text{N}$ 単一量子井戸活性層404を4nm厚、p- $\text{Al}_{0.1}\text{Ga}_{0.9}\text{N}$ 蒸発防止層405を0.1 μ m厚、p-GaNコンタクト層406を0.4 μ m厚成長させた。以上までに作製された発光素子の工程断面図を図5(b)に示す。

【0029】さらに、通常的光リソグラフィ技術とドライエッチング技術を用いて $\text{In}_{0.45}\text{Ga}_{0.55}\text{N}$ 単一量子井戸活性層404を含む300 μ m角メサ410を周期的に残し、その間の領域を100 μ m幅でエッチングし、n-GaN連続膜半導体層401をエッチング底

面に露出させた。すなわち、エッチングを行った領域は400 μ mピッチの格子状の形状となり、これにより、溝構造450の上にMBE成長された欠陥を多く含む溝構造450の直上領域451とその周辺に含まれる $\text{In}_{0.45}\text{Ga}_{0.55}\text{N}$ 単一量子井戸活性層404を完全に除去した。本実施の形態では溝構造450が成長抑制構造となる。以上までに作製された発光素子の工程断面図を図5(c)に示す。

【0030】次に、ウェハの裏面を研磨し、サファイア基板400を完全に除去しn-GaN連続膜半導体層401をウェハ裏面に露出させた後、このn-GaN連続膜半導体層401にn型電極407を、メサ410の表面に光透過性のp型電極408を形成した。最後に、溝構造450の直上領域451でスクライブすることにより、個々の発光ダイオードチップとした。以上までに作製された発光素子の工程断面図を図4に示す。

【0031】このようにして作製された発光ダイオードの電子の光子への変換効率を測定したところ、実用上問題がないとみなすことが出来る変換効率5%以上の素子の歩留まりが85%と高かった。さらに、本実施例素子を従来例素子と同様の条件にて信頼性試験を実施したところ、1000時間経過後においても、試験開始時の95~103%の発光強度を得ることができ、実用上問題のない信頼性が確保された。

【0032】本実施形態の発光素子における発光領域は、 $\text{In}_{0.45}\text{Ga}_{0.55}\text{N}$ 単一量子井戸活性層404が残存しているメサ410部に相当する。n-GaN連続膜半導体層401成長時に成長抑制構造として利用した溝構造450の直上領域451を除いた領域にメサ410が形成されているため、作製された全ての発光素子において発光領域には溝構造450の直上領域451は含まれていない。また、エッチングにより $\text{In}_{0.45}\text{Ga}_{0.55}\text{N}$ 単一量子井戸活性層404が除去された幅は100 μ mであり、メサ410部の発光領域は幅40 μ mの溝構造450の端から30 μ m離れたところに形成されていることとなる。上記のように発光効率の高い素子を歩留まり良く得ることができ、かつ問題のない信頼性を実現できるのは、HVPE法およびMOCVD法による結晶成長工程により溝構造450の直上領域451に集中的に導入された結晶欠陥の影響が、 $\text{In}_{0.45}\text{Ga}_{0.55}\text{N}$ 単一量子井戸活性層404での発光に悪影響を与えず、比較的結晶欠陥の少ない部分に制御性良く発光領域を配置することが可能となったためと考えられる。

【0033】なお、上記の実施形態の発光素子において、発光素子作製工程および構造はほぼ同等とし、溝構造450のピッチのみを上記の例の400 μ mから500 μ mおよび300 μ mに変化させた場合の発光素子を試作した。この場合においてもメサ410の大きさや作製ピッチはそれぞれ300 μ m、400 μ mと上記の実施形態素子のままとした。これらの発光素子の発光特性

を測定したところ、溝450のピッチを300 μm と小さくした素子では、5%以上の発光効率を得られる歩留まりは16%と激減した。一方、500 μm と広げた発光素子では38%であった。これは、溝構造450のピッチが、個々の発光ダイオードを形成するメサ410の作製ピッチと同一であることが重要であることを示している。従って、同一面積のウェハからより多くの発光素子を作製するためには、全ての発光素子において溝構造の直上領域451が発光領域に含有されないようにすべきである。この意味に置いて、溝構造450のピッチをメサ410作製ピッチの整数倍にしても良いことは言うまでもない。

【0034】(実施形態3)次に、成長抑制構造自体をレーザ素子に残存させた実施形態について説明する。図6に本実施形態の素子構造図を示す。本実施形態の素子構造はn-SiC基板600と、Ga_{0.9}Nバッファ層601、n-GaN連続膜半導体層602、n-GaNバッファ層603、n-Al_{0.1}Ga_{0.9}Nクラッド層604、3nm厚のIn_{0.1}Ga_{0.85}Al_{0.05}Nバリア層3層と3nm厚のIn_{0.2}Ga_{0.8}N量子井戸層2層からなる多重量子井戸活性層605、p-Al_{0.1}Ga_{0.9}Nクラッド層606、p-GaNコンタクト層607、からなる半導体層構造と、p型電極611、n型電極612、さらには、導波路と電流通路を規定するメサストライプ610、共振器ミラーとなるエッチドミラー613を有している。

【0035】以下に、本実施形態のレーザ素子の作製方法について説明する。(工程図は図2と類似しているのでここでは省略する。)まず、n-SiC基板600上に、SiN_xからなる幅10 μm で周期が100 μm の選択成長マスク650と、幅が10 μm で周期が400 μm の選択成長マスク651とが互いに直交するように形成した。このウェハ上にMOCVD法によりGa_{0.9}Nバッファ層601を30nm厚、n-GaN連続膜半導体層602を100 μm 厚、n-GaNバッファ層603を0.1 μm 厚、n-AlGa_{0.9}Nクラッド層604を0.3 μm 厚、多重量子井戸活性層605、p-AlGa_{0.9}Nクラッド層606を0.3 μm 厚、p-GaNコンタクト層607を1.0 μm 厚連続的に結晶成長させる。この時、n-GaN連続膜半導体層602の成長においては、厚さが30 μm 以下の状態では選択成長マスク650、651上では未成長部分が残存しており、結晶は連続した膜を呈していなかったが、さらに成長を続けて厚さが100 μm に達した段階では、n-GaN連続膜半導体層602表面は実施形態1と同様に平坦で連続した単膜を呈しており、その上に連続的に形成された積層構造に含まれる各層603~607もまた平坦な層として成長された。

【0036】次に、通常的光リソグラフィ技術とエッチング技術を利用し、高さ0.8 μm 、幅2 μm のメ

サストライプ610を選択成長マスク651と平行に形成した。このメサストライプ610はレーザ導波路を活性層605に形成するばかりでなく、活性層605に注入される電流の通路もメサストライプ610直下近傍部分に規定し、効率よく電子をレーザ光に変換する働きをする。本工程において、メサストライプ610は、両側の選択成長マスク651の直上領域653の中央、すなわち選択成長マスク651の端とメサストライプ610の端の間隔が39 μm となるように形成した。

【0037】次に、通常のエッチドミラー形成のためのフォトリソグラフィ技術とドライエッチング技術を利用し、レーザ共振器ミラーとなるエッチドミラー613を形成した。この時、エッチドミラー613が選択成長マスク650に平行であり、かつ選択成長マスク650の直上領域652の活性層605をエッチングより除去するように、選択成長マスク650の直上領域652を中心として全幅100 μm の領域にエッチングを施し、n-GaN連続膜半導体層602がエッチング底面に露出するまでエッチングを行った。この工程によりレーザ共振器となるべき一組の共振器ミラーが形成され、本実施形態のレーザ素子における共振器長は300 μm とした。すなわち、選択成長マスク650の周期と同じ400 μm 周期でエッチドミラー形成のためのエッチングを実施したことになる。

【0038】最後に、メサストライプ610上面にp型電極611を、n-SiC基板600裏面全面にn型電極612を形成した後、選択成長マスク650、651の直上領域652、653の部分でスクライプすることにより個々のレーザ素子に分割した。

【0039】本実施形態のレーザ素子を実施形態2の60°C雰囲気下、5mW光出力の条件下での信頼性試験を実施したところ、初期24時間の異常劣化を示した素子を除いて、全て1000時間以上の寿命を有することが確認できた。この場合のメディアン寿命は約1600時間であった。このように、信頼性の高いレーザが実現できたのは、選択成長マスク650の直上領域652が発光領域であるメサストライプ610に全く含まれず、レーザ素子の劣化を引き起こす結晶欠陥が少ない領域のみの活性層605が発光に寄与している効果と推察される。

【0040】ところで、実施形態1においてはレーザ素子の劈開位置は選択成長マスク150の直上領域152外の部分に限られていた。これは、選択成長マスク150の直上領域152で劈開した場合に、レーザの発光領域となるメサストライプ110内の破壊し易い劈開面近傍に結晶欠陥が多く含まれる選択成長マスクの直上領域152が包含され、素子を動作させた時に瞬時に劣化することを避けるためである。しかし、実施形態1におけるように選択成長マスク150の直上領域152の近傍にて選択成長マスク150の直上領域152に平行に

劈開をした場合、部分的に劈開面に段差が生じ、結果として一部の素子にてメサストライプ110に選択成長マスク150の直上領域152が含まれてしまう場合があった。これは、選択成長マスク150の直上領域152に結晶欠陥が多く含まれており、結晶として弱く、より割れやすいことが原因と考えられる。すなわち、選択成長マスク150の直上領域152で結晶が劈開しやすい性質を持ち合わせているのに関わらず、実施形態1ではその近傍を劈開していたためである。この現象は、劈開により素子を分割する場合のみならず、スクライブにより素子を分割する場合にも同様の現象が観測され、選択マスク151の直上領域153でスクライブした場合には比べて、選択マスク151の直上領域153近傍で選択マスク151の直上領域153と平行に制御性良くスクライブした場合の歩留まりは低かった。

【0041】一方、本実施形態素子では、素子を分割する際の4面全てのスクライブによる素子分割位置を選択成長マスク650、651の直上領域652、653に限定できるため、素子分割時に所定の位置にてスクライブが起こり、メサストライプ610に選択マスクの直上領域652が含まれたり、所定の形状（上方から観察して図6に示すように直方形）から素子の形状がずれることは無かった。これにより、素子をマウントする際の素子形状認識においても、エラーを低下させることができ、素子マウント歩留まりも改善することができた。この点も、本実施形態素子における大きなメリットであった。

【0042】（実施形態4）次に、成長抑制構造の直上領域の活性層が素子に残存している場合の本発明の実施形態を発光ダイオードの例を用いて説明する。図7に、本実施形態の発光素子の上面より観察した構造図を示す。Ga_{0.45}N連続膜層の形成方法や半導体積層構造は実施形態2の場合と同じとした（本実施形態例の説明では共通する各層の標記は実施例2と同一とする）。実施形態2と異なるのは、In_{0.45}Ga_{0.55}N単一量子井戸活性層404を含むメサ710の形状が図7のような形状を有しており、かつそのサイズを390μm角と大きくした点である。このため、本実施形態の発光素子では、n-GaN連続膜層401成長時の成長抑制構造たる溝構造450の直上領域751に位置するIn_{0.45}Ga_{0.55}N単一量子井戸活性層404がメサ710内に含まれた形となっている。

【0043】しかし、本実施形態の発光素子では、p型電極711を300μm角として、メサ710の中央領域に配置した。すなわち、溝構造450の直上領域751および直上領域751の端から30μmの領域においてはp型電極が形成されないようにした。一方、n型電極712はIn_{0.45}Ga_{0.55}N単一量子井戸活性層404が除去された発光素子の一角に図7のように形成した。

【0044】このような構成とすることにより、p型コンタクト層406、p型電極711から注入される電流はp-GaNコンタクト層406が、比較的抵抗率の高いp-GaNからなっており、かつ0.4μmとその膜厚が薄いために、p型コンタクト層406中ではほとんど電流が横方向に拡散せず、p型電極711の直下のIn_{0.45}Ga_{0.55}N単一量子井戸活性層404にのみ電流を注入することができる。

【0045】当該実施形態の発光素子の特性を評価した結果、5%以上の電子-光子変換効率を有するチップは、検査した内の79%に達し、従来技術により構成された発光素子より格段の改善が認められた。また、これらの発光素子の信頼性試験（条件は実施形態2と同様）を行ったところ、1000時間経過後の発光輝度は試験当初の発光輝度に対して85~99%の範囲となり、全ての発光素子が実用上問題ないことが確認された。

【0046】以上、実施形態の発光素子においては、Ga_{0.45}N連続膜半導体層を用いて窒化ガリウム系の発光素子を作製した例を説明したが、本発明は以下のような場合にも適用できることはいうまでもない。

（1）基板材料や連続膜半導体層の材料、および発光素子を構成する材料が異なる場合（例えば、基板がSi、連続膜半導体層がGaAs、の場合や基板がSi、GaAsで連続膜層がGaNである場合、等）。

（2）成長抑制構造である選択成長マスクの材料が異なる場合（SiN_x、SiO_x、AlO_x、等）や、構造自体が選択成長マスクや溝構造以外の場合（例えば、サファイア基板上に形成したリッジストライプやその他の凹凸構造、等）。

（3）連続膜半導体層を形成後、発光層形成前に基板を完全に除去するように工程の順番を変更した場合。

【0047】

【発明の効果】以上のように、本発明を適用することにより、基板とは格子定数や熱膨張係数が異なる連続膜半導体層上に半導体発光素子を作製した場合、発光効率の低下を防止し、歩留まり良く発光効率の高い発光ダイオードや半導体レーザを実現できた。また、本発明により、これらの発光素子において実用上十分な信頼性を確保することが可能となった。

【図面の簡単な説明】

【図1】本発明の実施の形態1の半導体レーザ素子の断面図である。

【図2】本発明の実施の形態1の半導体レーザ素子の作製工程図である。

【図3】成長マスクの直上領域からメサストライプまでの距離に対するメディア寿命を示す図である。

【図4】本発明の実施の形態2の半導体発光素子の断面図である。

【図5】本発明の実施の形態2の半導体発光素子の作製工程図である。

【図6】本発明の実施の形態3の半導体レーザ素子の断面図である。

【図7】本発明の実施の形態4の半導体発光素子の上面図である。

【図8】従来の半導体発光素子の作製工程図である。

【図9】従来の半導体発光素子の構造を示す図である。

【図10】成長抑制構造からの距離に対する結晶転移の面密度を示す図である。

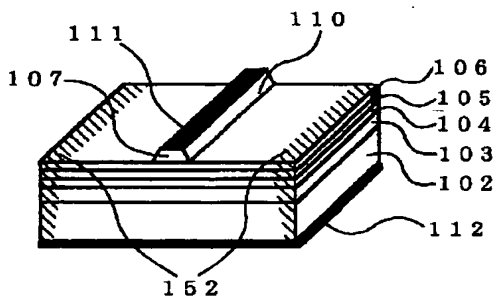
【符号の説明】

100 サファイア基板
101、601 GaNバッファ層
102、602、401 n-GaN連続膜層
103、603、402 n-GaNバッファ層
104、604 n-Al_{0.1}Ga_{0.9}Nクラッド層
105、605 多重量子井戸活性層
106、606、405 p-Al_{0.1}Ga_{0.9}Nクラッド層

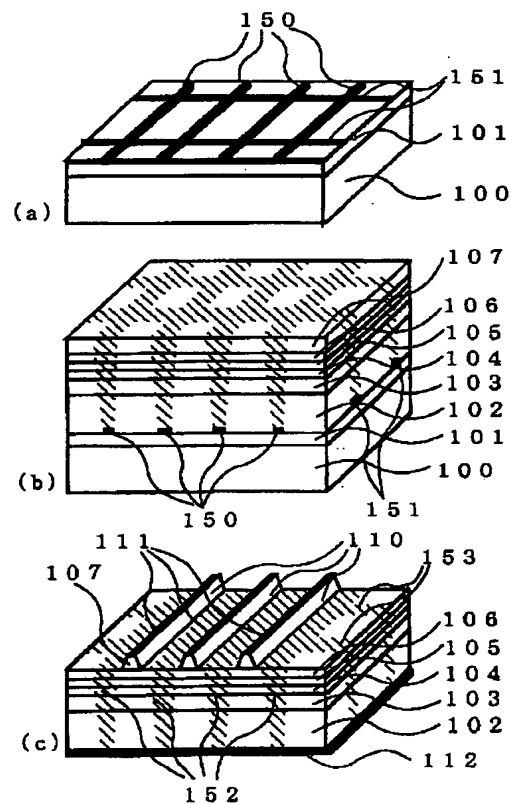
ド層

107、607 406 p-GaNコンタクト層
110、610 メサストライプ
111、611、408、711 p型電極
112、612、407、712 n型電極
150、151、650、651 選択成長マスク
152、153、652、653 直上領域
400 サファイア基板
403 In_{0.2}Ga_{0.8}N歪み緩和層
404 In_{0.45}Ga_{0.55}N単一量子井戸活性層
410 メサ
450 溝構造
451、751 直上領域
600 SiC基板
710 メサ

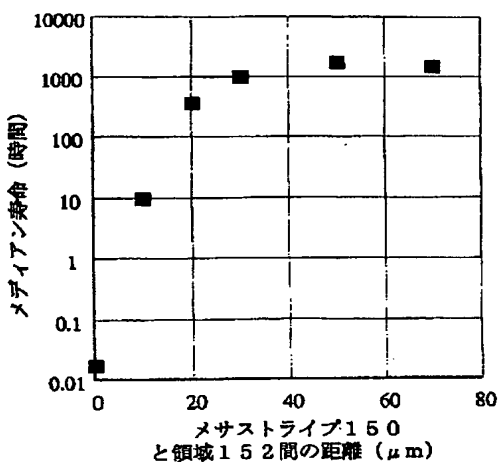
【図1】



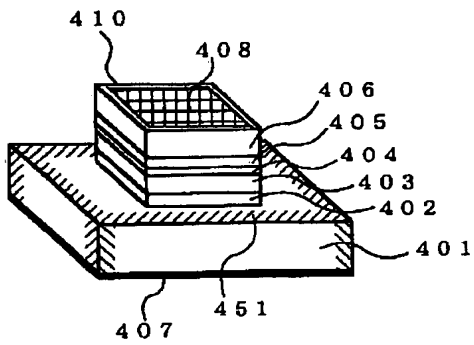
【図2】



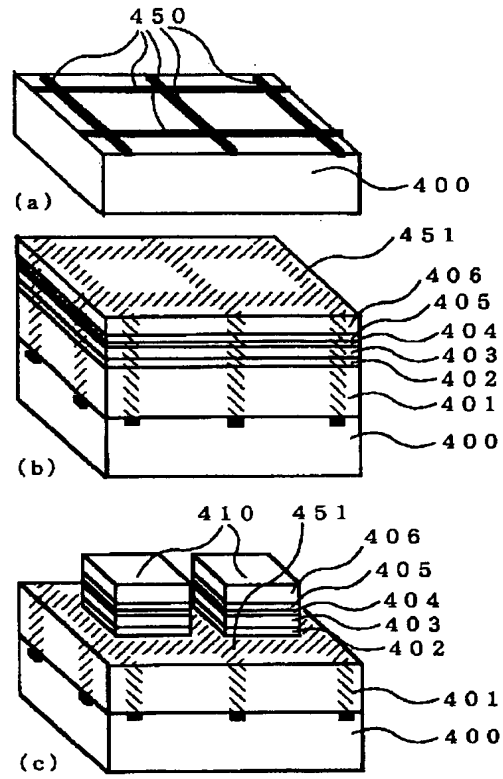
【図3】



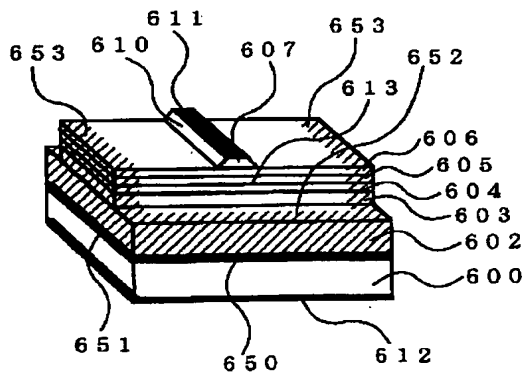
【図4】



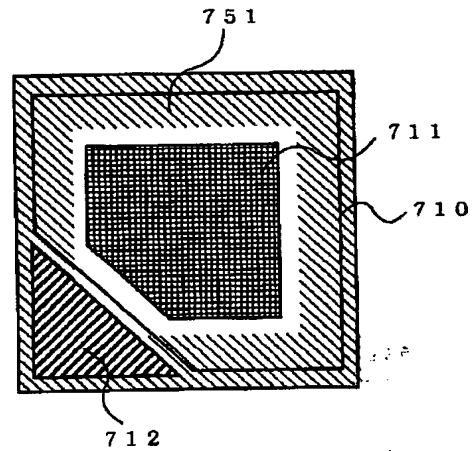
【図5】



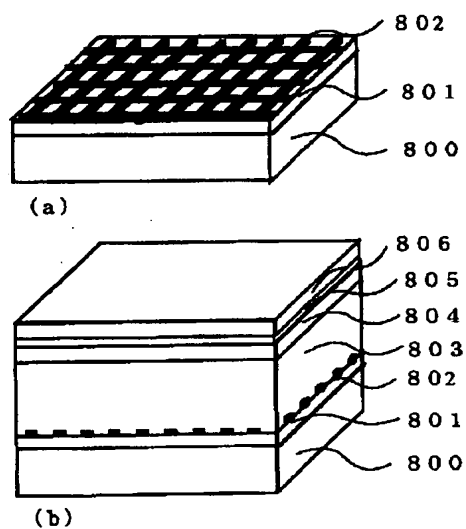
【図6】



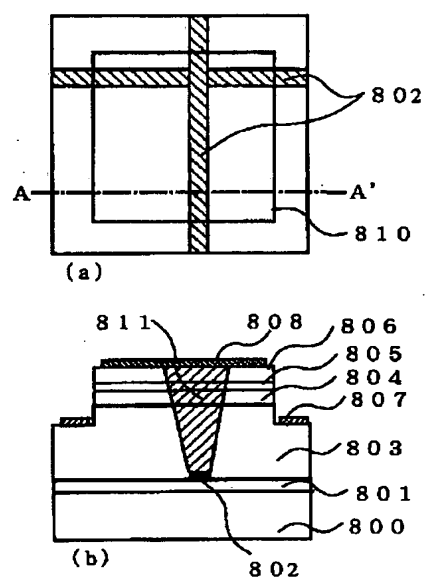
【図7】



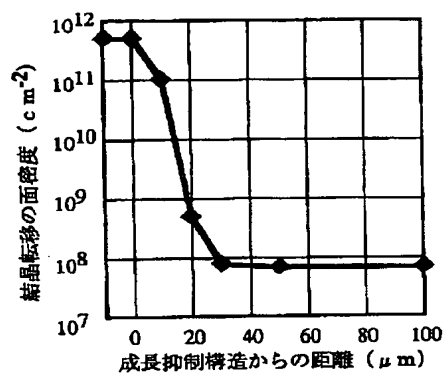
【図8】



【図9】



【図10】



*** NOTICES ***

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CLAIMS

[Claim(s)]

[Claim 1] The semi-conductor light emitting device characterized by forming in fields other than said growth suppression structure right above field the luminescence field which is the semi-conductor light emitting device which has a continuation film semi-conductor layer including the growth suppression structure right above field obtained with the crystal growth to a growth suppression structure top, and the barrier layer which generates light, and generates light by current impregnation among these barrier layers.

[Claim 2] Said luminescence field is a semi-conductor light emitting device according to claim 1 characterized by being formed in the location which separated 30 micrometers or more from the growth suppression structure right above field.

[Claim 3] The semi-conductor light emitting device characterized by removing said barrier layer in the field between said luminescence field and said growth suppression structure right above field.

[Claim 4] The 1st process which forms growth suppression structure on a substrate, and the 2nd process which forms the continuation film semi-conductor layer from which said substrate and lattice constant, or a coefficient of thermal expansion differs so that both said substrate and said growth suppression structure may be covered continuously, The manufacture approach of the semi-conductor light emitting device characterized by having the 3rd process which forms the multilayer-structure object containing the barrier layer which generates light on said continuation film semi-conductor layer, and the 4th process which forms the structure for specifying the luminescence field in said barrier layer except for the right above field of said growth suppression structured division.

[Claim 5] The manufacture approach of the semi-conductor light emitting device according to claim 4 which is the manufacture approach of a semi-conductor light emitting device of having the process which divides a semi-conductor light emitting device into two or more semi-conductor light emitting devices from a wafer, and is characterized by including the 5th process which divides a semi-conductor light emitting device from a wafer so that said barrier layer of said growth suppression structure right above may not be contained in a semi-conductor light emitting device after said 4th process.

[Claim 6] The manufacture approach of a semi-conductor light emitting device according to claim 5 that said barrier layer which remains from the edge of said growth suppression structure right above to a less than 30-micrometer field is characterized by dividing a semi-conductor light emitting device so that it may not be contained in a semi-conductor light emitting device in said 5th process.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a semi-conductor light emitting device with the high dependability formed on the substrate with the semiconductor material with which a lattice constant or a coefficient of thermal expansion differs especially from a substrate about a semi-conductor light emitting device.

[0002]

[Description of the Prior Art] When forming in up to the substrate with which a lattice constant differs from the crystal ingredient which constitutes a semi-conductor light emitting device 3% or more, or when growing up a semiconducting crystal to be up to the substrate with which coefficients of thermal expansion differ 10% or more, the attempt which the ingredient which constitutes a semi-conductor light emitting device, and the crystal ingredient with almost equal (a lattice constant and a coefficient of thermal expansion less than 1%) a lattice constant and a coefficient of thermal expansion were grown up thickly, formed the continuation film semi-conductor layer upwards on the substrate first, and forms a semi-conductor light emitting device is made. It is reported that a crystal defect reduces the semi-conductor layer which carried out the laminating on the continuation film semi-conductor layer. The example by the conventional technique which was made to carry out crystal growth of the GaN layer thickly, formed the continuation film semi-conductor layer on silicon on sapphire 800, and formed blue light emitting diode (LED) on it as an example of representation of such a light emitting device at drawing 8 is shown.

[0003] The production approach of LED of this conventional example is explained. On silicon on sapphire 800, the GaN layer 801 is first grown up into 5-micrometer thickness thickly by halide vapor growth (HVPE law). Next, the selective growth mask 802 which consists of SiO₂ is formed in GaN layer 801 front face in the shape of a grid (form where SiO₂ stripe of 20-micrometer width of face of 200-micrometer pitch intersects perpendicularly mutually). The process sectional view produced by the above is shown in drawing 8 (a).

[0004] next, this silicon-on-sapphire 800 top -- HVPE -- 300-micrometer thickness growth of the n mold GaN continuation film semi-conductor layer 803 is carried out by law. It grew up to be also right and left so that the n mold GaN continuation film semi-conductor layer 803 which grew according to the HVPE process at this time might be jugged out to up to the mask 802 for selective growth which that thickness follows on increasing and consists of SiO₂, although growth begins from the part which silicon on sapphire 800 exposed, and the selective growth mask 802 top which finally consists of SiO₂ of 20-micrometer width of face was covered. Thus, the n mold GaN continuation film semi-conductor layer 803 with a flat front face was formed.

[0005] Next, the n-GaN cladding layer 804, the InGaN barrier layer 805, and the p-GaN contact layer 806 were formed in the wafer with which the n mold GaN continuation film semi-conductor layer 803 was formed on this silicon on sapphire 800 of metal-organic chemical vapor deposition (MOCVD) law. The process sectional view produced by the above is shown in drawing 8 (b).

[0006] Next, as shown in top-face structural drawing of LED of the (a) conventional example of drawing 9, and the A-A' sectional view of the (b) conventional example LED, it left the luminescence field 810 of 300-micrometer angle, and it removed so that the surroundings of it might be surrounded, and the p-GaN contact layer 806, the InGaN barrier layer 805, and the n-GaN cladding layer 804 might be penetrated using a usual photolithography technique and a usual dry etching technique, and the n mold GaN continuation film semi-conductor layer 803 was exposed. Finally, p mold electrode 808 which has n

mold electrode 807 on the front face of the n mold GaN continuation film semi-conductor layer 803, and has light transmission nature on the front face of the p-GaN contact layer 806 of 300-micrometer angle was formed, respectively. Thus, from the produced wafer, the scribe was carried out around the luminescence field 810, and each LED was started and it considered as the component. Thus, LED of the conventional example to produce is reported.

[0007]

[Problem(s) to be Solved by the Invention] However, the result to which the artificer concerned examined the property of LED which carried out in this way and was produced, The luminous efficiency (conversion efficiency to an electronic photon) at the time of pouring in a 20mA current differs from 0.3 to 10% greatly by each component. It newly became clear that the yield from which 5% or more of desired luminous efficiency is acquired is very as low as 2%, and that the luminous efficiency of all components decreased sharply to about 30% or less at the time of test initiation in the initial reliability trial of about 100 hours under 80-degree C conditions.

[0008] As a result of performing these examination with the artificer concerned detailed about the defect of a component conventionally, the following facts became clear.

(1) Luminescence in InGaN barrier layer 805 part located in the selective growth mask right above field 811 to which the selective growth mask 802 exists is very small. Moreover, when the selective growth mask right above field 811 was located in the central field of the luminescence field 810 from the boundary region of the luminescence field 810 of a chip, it also turned out that the decline in this luminous efficiency becomes remarkable especially. Thereby, luminous efficiency changes a lot by whether the selective growth mask right above field 811 is located in the part of luminescence field 810 throat.

(2) Also in the component of above-mentioned poor dependability, as for the InGaN barrier layer 805 of the selective growth mask right above field 811 (width of face of 20 micrometers), luminescence is hardly accepted after reliability-trial transit of 100 hours at a total of a 80-micrometer field including about 30 micrometers of both sides of the near.

[0009] As a result of performing crystal analysis of the conventional example component furthermore, it became clear that penetrate the n mold GaN continuation film semi-conductor layer 803 with a thickness of 300 micrometers, and crystal transition concentrates and is introduced into the InGaN barrier layer 805 located in the selective growth mask right above field 811. The result of having measured the distance from selective growth mask 802 edge for the consistency of the crystal transition in the InGaN barrier layer 805 as a parameter to drawing 10 is shown. Crystal transition of consistency 10^{12}cm^{-2} was concentrating on the InGaN barrier layer 805 of the selective growth mask right above field 811 with a width of face of 20 micrometers, and transition of 10^{11}cm^{-2} was observed also in the location which separated 10 micrometers from the edge of the selective growth mask 802 further. Crystal transition decreased as it separated from the edge of the selective growth mask 802, and in the InGaN barrier layer 805 of the location distant 30 micrometers or more, crystal transition decreased even to $10^7\text{--}10^8\text{cm}^{-3}$. Such an inclination was observed in any part of the wafer produced as mentioned above.

[0010] Moreover, the selective growth mask right above field 811 was included in the luminescence field in semiconductor laser by the same approach on the above n mold GaN continuation film semi-conductor layers 803, it was as large as 700mA, and the component life also had the oscillation threshold current very as short as about 1 second in the room temperature.

[0011] As mentioned above, in the conventional technique, the following troubles became clear.

(1) In the light emitting device on the continuation film semi-conductor layer produced using the selection grown method, since decline in luminous efficiency is seen in the selective growth mask right above field 811, with the chip in which a selective growth mask right above field is included, luminous efficiency falls to a luminescence field dramatically.

(2) The life of the semiconductor laser component formed on the GaN continuation film was short, and the semiconductor laser component was not obtained.

[0012] For this reason, it was impossible to have prevented a fall and poor dependability of the luminous efficiency caused in the semi-conductor light emitting device which the continuation film semi-conductor layer which has a different lattice constant from a substrate and a coefficient of thermal expansion is grown up, and is formed on it on a substrate from a lattice constant difference or a coefficient-of-thermal-expansion difference.

[0013] Therefore, it aims at preventing the decline in the luminous efficiency in the case of having formed upwards the continuation film semi-conductor layer from which a substrate, a lattice constant,

or a coefficient of thermal expansion differs using partial growth suppression structure, and forming a semi-conductor light emitting device further, and aggravation of dependability.

[0014]

[Means for Solving the Problem] Claim 1 of this invention is constituted by forming in fields other than said growth suppression structure right above field the luminescence field which is the semi-conductor light emitting device which has a continuation film semi-conductor layer including the growth suppression structure right above field obtained with the crystal growth to a growth suppression structure top, and the barrier layer which generates light, and generates light by current impregnation among these barrier layers.

[0015] Claim 2 in this invention is constituted by being formed in the location where said luminescence field separated 30 micrometers or more from the growth suppression structure right above field, and claim 3 consists of fields between said luminescence field and said growth suppression structure right above field for it by removing said barrier layer further.

[0016] The 1st process at which claim 4 forms growth suppression structure on a substrate on the other hand, and the 2nd process which forms the continuation film semi-conductor layer from which said substrate and lattice constant, or a coefficient of thermal expansion differs so that both said substrate and said growth suppression structure may be covered continuously, The 3rd process which forms the multilayer-structure object containing the barrier layer which generates light on said continuation film semi-conductor layer, It is constituted by having the 4th process which forms the structure for specifying the luminescence field in said barrier layer except for the right above field of said growth suppression structured division. Further claim 5 It is the manufacture approach of a semi-conductor light emitting device of having the process which divides a semi-conductor light emitting device into two or more semi-conductor light emitting devices from a wafer. After said 4th process, are constituted by including the 5th process which divides a semi-conductor light emitting device from a wafer so that said barrier layer of said growth suppression structure right above may not be contained in a semi-conductor light emitting device, and claim 6 is set at said 5th process. Said barrier layer which remains from the edge of said growth suppression structure right above to a less than 30-micrometer field is constituted by dividing a semi-conductor light emitting device so that it may not be contained in a semi-conductor light emitting device.

[0017]

[Embodiment of the Invention] It explains using the example which carried out this invention below. (Gestalt 1 of operation) An example of a semiconductor laser component which carried out this invention to drawing 1 is shown. This semiconductor laser component consists of the n-GaN continuation film semi-conductor layer 102, the n-GaN buffer layer 103, the n-aluminum0.1Ga0.9N cladding layer 104, a multiplex quantum well barrier layer 105, a p-aluminum0.1Ga0.9N cladding layer 106, and a p-GaN contact layer 107, and consists of a mesa stripe 110 for specifying the luminescence field of laser as a ridge waveguide, a p mold electrode 111 further for current impregnation, and an n mold electrode 112.

[0018] Next, the making process of this example component is explained using drawing 2. first, a silicon-on-sapphire 100 top -- MOCVD -- 1-micrometer thickness growth of the GaN buffer layer 101 is carried out by law. next, the usual photolithography technique after carrying out 0.4-micrometer thickness formation of the SiO₂ film by the usual spatter on the front face of the GaN buffer layer 101 and an etching technique -- width of face of 10 micrometers -- pitch 150micrometer -- periodic -- the selective growth mask 150 and width of face of 10 micrometers which consist of SiO₂ -- pitch 500micrometer -- periodic -- the selective growth mask 151 which consists of SiO₂ formed in the configuration which intersects perpendicularly mutually. The process sectional view of the semiconductor laser component produced by the above is shown in drawing 2 (a).

[0019] then, this wafer top -- HVPE -- 150-micrometer thickness growth of the n-GaN continuation film semi-conductor layer 102 was carried out by law. Growth of 150-micrometer thickness completed substrate temperature with the growth for 35 minutes as 1020 degrees C. In the phase which growth took place only in the field which the GaN buffer film 101 exposed in early stages of growth like explanation in the conventional example in order that the selective growth masks 150 and 151 might work as growth suppression structure at the time of this growth, growth progressed in the longitudinal direction on the selective growth mask 150 and 151 gradually, and growth of 150 micrometer thickness finally ended, the n-GaN continuation film semi-conductor layer 102 is presenting the continuation film, and that front face became smooth.

[0020] By the MOCVD method, succeedingly next, on this n-GaN continuation film semi-conductor layer

102 0.5-micrometer thickness and the n-aluminum0.1Ga0.9N cladding layer 104 for the n-GaN buffer layer 103 0.2-micrometer thickness, The multiplex quantum well barrier layer 105 and the p-aluminum0.1Ga0.9N cladding layer 106 which consist of In0.25Ga0.75N well layer two-layer of 4nm thickness, and three layers of In0.05Ga0.95N barrier layers of 3nm thickness 0.2-micrometer thickness, 0.7-micrometer thickness growth of the p-GaN contact layer 107 was carried out. The process sectional view of the semiconductor laser component produced by the above is shown in drawing 2 (b). [0021] Then, the mesa stripe 110 with a width of face [of 2 micrometers] and a height of 0.7 micrometers was formed in fields other than right above field 152 of the selective growth mask 150 almost in parallel with the selective growth mask 150. the selective growth mask 150 with which the mesa stripe 110 observes and adjoins each other from the upper part of a component at this time -- it was made to be mostly located in the center A usual photolithography technique and a usual dry etching technique were applied to formation of this mesa stripe 110. Then, after forming stripe-like p mold electrode 111 in a top face for the mesa stripe 110, Wafer thickness is set to about 120 micrometers by grinding a wafer rear face (). Namely, silicon on sapphire 100, the GaN buffer layer 101, and the selective growth masks 150 and 151 are removed completely. The n-GaN continuation film semi-conductor layer 102 formed n mold electrode 112 all over the rear face which it is made to expose to a wafer rear face, and the n-GaN continuation film semi-conductor layer 102 exposed. The process sectional view of the semiconductor laser component produced by the above is shown in drawing 2 (c).

[0022] Next, the mirror side which constitutes a laser cavity by cleavage was formed. This cleavage process is the following, and was made and carried out. First, the marking-off blemish was put into two near [on the rear face of a wafer (namely, the n-GaN continuation membrane layer 103 side)] the corner, cleavage was carried out to the direction and the parallel direction in which the selective growth mask 151 was formed, in the location of this marking-off blemish, and the laser resonator mirror was formed. At this time, two marking-off blemishes are formed in the location which separated 50 micrometers from the edge part of the selective growth mask 151 which adjoins mutually, and the right above field 153 of the selective growth mask 151 was made not to be included in a laser component. Therefore, laser cavity length was 400 micrometers. The scribe of the part of the right above field 152 of the selective growth mask 150 was carried out to the last, and it divided into each laser chip. The laser component shown in drawing 1 through the above process is completed.

[0023] The laser component produced as mentioned above has realized laser oscillation by the threshold current of 25mA. Moreover, except for the laser component which results this laser component within 50 hours of the first stage at failure as a result of carrying out a reliability trial under 50-degree-C ambient atmosphere and the condition of 3mW output, the life of 1000 hours or more could be checked in almost all components, and the median life (time amount to which the component of the examined one half breaks down) was 1500 hours. This dependability is sufficient property even when using the component concerned as the light source for optical disks. An improvement of this dependability with this laser component In selective growth mask [which is the growth suppression structure formed in order to grow up the n-GaN continuation film semi-conductor layer 102] 150, and 151 top So that the right above fields 152 and 153 which a crystal defect concentrates may not be included to the luminescence field (in this case, part in which the mesa stripe 110 with which a current is alternatively poured into a barrier layer 105 is formed) of a laser component It can be understood as what is depended on having set up the relative position for the configuration of the selective growth masks 150 and 151, and the cleavage of a laser resonator mirror to the relative position and the selective growth mask 151 of the mesa stripe 110 to the selective growth mask 150.

[0024] With the laser component which carried out the above-mentioned invention, it is formed so that it may become the center of right above field 152 comrades of the selective growth mask 150 which adjoins the mesa stripe 110 (into namely, part which separated 70 micrometers from the edge of the selective growth mask 150). With the same structure as the above-mentioned example component, the laser component to which the distance from right above field 152 (namely, selective growth mask 150) edge of the mesa stripe 110 was changed with 0 micrometer, 10 micrometers, 20 micrometers, 30 micrometers, 50 micrometers, and 70 micrometers (namely, when the mesa stripe 110 is formed in the right above field 152) was produced, and the same reliability trial as the above was carried out. At this time, the scribe location of an isolation sake was made into near the core of the mesa stripe 110 which adjoins also in which component, and set constant the relative distance with the mesa stripe 110 of a scribe location. The result is shown in drawing 3. An axis of abscissa shows the distance from the core of the right above field 152 to the mesa stripe 110, and the axis of ordinate shows the median life. In order to secure from this result the median life of 1000 hours or more needed practically, it turned out

that it is required to form the mesa stripe 110 in the location which separated 30 micrometers or more from the right above field 152.

[0025] (Gestalt 2 of operation) Next, the case where this invention is applied to light emitting diode is described. Structural drawing of the 2nd operation morphological child is shown in drawing 4. It consists of the n-GaN continuation film semi-conductor layer 401, the n-GaN buffer layer 402, the In_{0.1}Ga_{0.9}N strain relaxation layer 403, the In_{0.5}Ga_{0.5}N single quantum well barrier layer 404, the p-aluminum_{0.2}Ga_{0.8}N antilashing layer 405, a p-GaN contact layer 406 and an n mold electrode 407, and a p mold electrode 408. Moreover, the luminescence field is specified by the mesa 410 with the component of this example.

[0026] Next, the production approach of this light emitting device is explained. First, the slot structure 450 with a width of face [of 40 micrometers] and a depth of 50 micrometers is formed in silicon-on-sapphire 400 front face in the shape of a grid in 400-micrometer pitch by dicing. The process sectional view of the semiconductor device produced by the above is shown in drawing 5 (a).

[0027] Next, by the HVPE method, the n-GaN continuation film semi-conductor layer 401 with a thickness of 300 micrometers is grown up. Although the growth as a flat field cannot do the n-GaN continuation film semi-conductor layer 401 in the early stages of growth since there is slot structure 450 formed in silicon on sapphire 400 at this time, the slot structure 450 will be gradually buried with the growth from a wall on either side as growth thickness is increased, and the slot on surface will be embedded evenly. That is, the same effectiveness as a thing with slow growth in a slot 450 could be realized effectually, and the continuous front face was able to use the n-GaN continuation membrane layer 401 as the flat single layer at the time of 300-micrometer growth termination.

[0028] next, molecular-beam epitaxial ** (MBE law) -- on the n-GaN continuation film semi-conductor layer 401, 0.05-micrometer thickness and the In_{0.45}Ga_{0.55}N single quantum well barrier layer 404 were carried out for 0.4-micrometer thickness and the In_{0.2}Ga_{0.8}N strain relaxation layer 403, and 0.4-micrometer thickness growth of 0.1-micrometer thickness and the p-GaN contact layer 406 was carried out [the n-GaN buffer layer 402] for 4nm thickness and the p-aluminum_{0.1}Ga_{0.9}N antilashing layer 405. The process sectional view of the light emitting device produced by the above is shown in drawing 5 (b).

[0029] Furthermore, it left periodically 300-micrometer angle mesa 410 which contains the In_{0.45}Ga_{0.55}N single quantum well barrier layer 404 using a usual photolithography technique and a usual dry etching technique, the field in the meantime was etched by 100-micrometer width of face, and the n-GaN continuation film semi-conductor layer 401 was exposed on the etching base. That is, the etched field became the configuration of the shape of a grid of 400-micrometer pitch, and the right above field 451 of the slot structure 450 which includes by this many defects by which MBE growth was carried out on the slot structure 450, and the In_{0.45}Ga_{0.55}N single quantum well barrier layer 404 contained around it were removed completely. With the gestalt of this operation, the slot structure 450 turns into growth suppression structure. The process sectional view of the light emitting device produced by the above is shown in drawing 5 (c).

[0030] Next, the rear face of a wafer was ground, after removing silicon on sapphire 400 completely and exposing the n-GaN continuation film semi-conductor layer 401 at the wafer rear face, n mold electrode 407 was formed in this n-GaN continuation film semi-conductor layer 401, and p mold electrode 408 of light transmission nature was formed in the front face of a mesa 410. It considered as each light emitting diode chip by carrying out a scribe to the last in the right above field 451 of the slot structure 450. The process sectional view of the light emitting device produced by the above is shown in drawing 4.

[0031] Thus, the yield of the component of **, alias *****, and 5% or more of conversion efficiency it can consider that is satisfactory practically was as high as 85% in the conversion efficiency to the photon of the electron of the produced light emitting diode. Furthermore, when the reliability trial was carried out for this example component on the same conditions as the conventional example component, 95 - 103% of luminescence reinforcement at the time of test initiation could be obtained after 1000-hour progress, and the dependability which is satisfactory practically was secured.

[0032] The luminescence field in the light emitting device of this operation gestalt is equivalent to the mesa 410 section in which the In_{0.45}Ga_{0.55}N single quantum well barrier layer 404 remains. Since the mesa 410 is formed in the field except the right above field 451 of the slot structure 450 used as growth suppression structure at the time of n-GaN continuation film semi-conductor layer 401 growth, in no produced light emitting devices, the right above field 451 of the slot structure 450 is included in the luminescence field. Moreover, the width of face from which the In_{0.45}Ga_{0.55}N single quantum well

barrier layer 404 was removed by etching is 100 micrometers, and the luminescence field of the mesa 410 section will be formed in the place which separated 30 micrometers from the edge of the slot structure 450 with a width of face of 40 micrometers. the dependability which can obtain a component with luminous efficiency high as mentioned above with the sufficient yield , and be satisfactory be realizable -- HVPE -- law and MOCVD -- the effect of the crystal defect intensively introduced into the right above field 451 of the slot structure 450 by the crystal growth process by law do not have a bad influence on luminescence by the $\text{In}_{0.45}\text{Ga}_{0.55}\text{N}$ single quantum well barrier layer 404 , but be consider because it became possible to arrange a luminescence field with a controllability sufficient into a part with comparatively few crystal defects .

[0033] In addition, in the light emitting device of the above-mentioned operation gestalt, a light emitting device making process and structure presupposed that it is almost equivalent, and made the light emitting device at the time of changing only the pitch of the slot structure 450 from 400 micrometers of the above-mentioned example to 500 micrometers and 300 micrometers as an experiment. Also in this case, the magnitude and the production pitch of a mesa 410 were considered as as [300 micrometers 400 micrometers, and the above-mentioned operation morphological child], respectively. When the luminescence property of these light emitting devices was measured, with the component which made the pitch of a slot 450 small with 300 micrometers, the yield from which 5% or more of luminous efficiency is acquired decreased sharply with 16%. On the other hand, in 500 micrometers and the opened light emitting device, it was 38%. This shows that it is important that the pitch of the slot structure 450 is the same as the production pitch of the mesa 410 which forms each light emitting diode. Therefore, in order to produce many light emitting devices from the wafer of the same area, it should be made for the right above field 451 of slot structure not to contain to a luminescence field in all light emitting devices. It cannot be overemphasized that it may put on this semantics and the pitch of the slot structure 450 may be made into the integral multiple of a mesa 410 production pitch.

[0034] (Operation gestalt 3) Next, the operation gestalt which made the growth suppression structure itself remain for a laser component is explained. Component structural drawing of this operation gestalt is shown in drawing 6 . The component structure of this operation gestalt The n-SiC substrate 600, The GaN buffer layer 601, the n-GaN continuation film semi-conductor layer 602, The multiplex quantum well barrier layer 605 which consists of the n-GaN buffer layer 603, three layers of $\text{In}_{0.1}\text{Ga}_{0.85}\text{Al}_{0.05}\text{N}$ barrier layers of 604 or 3nm thickness of n-aluminum $0.1\text{Ga}_{0.9}\text{N}$ cladding layers, and $\text{In}_{0.2}\text{Ga}_{0.8}\text{N}$ quantum well layer two-layer of 3nm thickness, the p-aluminum $0.1\text{Ga}_{0.9}\text{N}$ cladding layer 606 and the p-GaN contact layer 607 -- since -- it has the becoming semi-conductor layer structure, p mold electrode 611 and n mold electrode 612, the mesa stripe 610 which specifies waveguide and a current path further, and the etched mirror 613 used as a resonator mirror.

[0035] Below, the production approach of the laser component of this operation gestalt is explained. (Since process drawing is similar with drawing 2 , it is omitted here.) First, on the n-SiC substrate 600, it formed so that the selective growth mask 650 whose period is 100 micrometers, and the selective growth mask 651 whose period width of face is 400 micrometers in 10 micrometers might intersect perpendicularly mutually by width of face of 10 micrometers which consists of SiN_x . this wafer top -- MOCVD -- law -- the GaN buffer layer 601 -- 30nm thickness and the n-GaN continuation film semi-conductor layer 602 -- 100-micrometer thickness and the n-GaN buffer layer 603 -- 0.1 micrometers and the n-AlGaIn cladding layer 604 -- 0.3-micrometer thickness, the multiplex quantum well barrier layer 605, and the p-AlGaIn cladding layer 606 -- 0.3-micrometer thickness and the p-GaN contact layer 607 -- 1.0-micrometer thickness -- crystal growth is carried out continuously. Although thickness remained in the condition 30 micrometers or less, the non-grown up part remained on the selective growth mask 650 and 651 and the crystal was not presenting the continuous film in growth of the n-GaN continuation film semi-conductor layer 602 at this time In the phase in which growth was furthermore continued and thickness amounted to 100 micrometers, the single film which was flat like the operation gestalt 1 as for n-GaN continuation film semi-conductor layer 602 front face, and continued is presented, and each class 603-607 contained in the laminated structure continuously formed on it also grew as a flat layer.

[0036] Next, a usual photolithography technique and a usual etching technique were used, and the mesa stripe 610 with a height [of 0.8 micrometers] and a width of face of 2 micrometers was formed in parallel with the selective growth mask 651. This mesa stripe 610 not only forms laser waveguide in a barrier layer 605, but specifies the path of the current poured into a barrier layer 605 into the part near directly under [mesa stripe 610], and it serves to change an electron into a laser beam efficiently. In this process, the mesa stripe 610 was formed so that spacing of the center of the right above field 653

of the selective growth mask 651 of both sides, i.e., the edge of the selective growth mask 651 and the edge of the mesa stripe 610, might be set to 39 micrometers.

[0037] Next, the photolithography technique and dry etching technique for the usual etched mirror formation were used, and the etched mirror 613 used as a laser resonator mirror was formed. At this time, the etched mirror 613 was parallel to the selective growth mask 650, and it etched until it etched into the field with a full of 100 micrometers centering on the right above field 652 of the selective growth mask 650 and the n-GaN continuation film semi-conductor layer 602 was exposed to the etching base so that the barrier layer 605 of the right above field 652 of the selective growth mask 650 might be removed from etching. The resonator mirror of a lot which should serve as a laser cavity according to this process was formed, and the cavity length in the laser component of this operation gestalt could be 300 micrometers. That is, it means carrying out etching for etched mirror formation in a cycle of [as the period of the selective growth mask 650 / same] 400 micrometer.

[0038] Finally, after forming p mold electrode 611 in mesa stripe 610 top face and forming n mold electrode 612 all over n-SiC substrate 600 rear face, it divided into each laser component by carrying out a scribe in the part of the right above fields 652 and 653 of the selective growth masks 650 and 651.

[0039] When the reliability trial under the conditions of 5mW optical output was carried out for the laser component of this operation gestalt under 60-degree-C ambient atmosphere of the operation gestalt 2, except for the component which showed abnormality degradation of initial 24 hours, it has checked having the life of 1000 hours or more altogether. The median life in this case was about 1600 hours. Thus, it is not included in the mesa stripe 610 whose right above field 652 of the selective growth mask 650 is a luminescence field at all that reliable laser was realizable, but it is imagined to be the effectiveness which the barrier layer 605 of only a field with few crystal defects which cause degradation of a laser component has contributed to luminescence.

[0040] By the way, in 1 of an operation gestalt, the cleavage location of a laser component was restricted to the part outside the right above field 152 of the selective growth mask 150. This is for avoiding deteriorating in an instant, when cleavage is carried out in the right above field 152 of the selective growth mask 150, the right above field 152 of the selective growth mask with which many crystal defects are included near the cleavage plane which it tends to destroy in the mesa stripe 110 used as the luminescence field of laser is included and a component is operated. However, when cleavage was carried out near the right above field 152 of the selective growth mask 150 as in the operation gestalt 1 in parallel with the right above field 152 of the selective growth mask 150, the level difference arose in the cleavage plane partially, and there was a case where the right above field 152 of the selective growth mask 150 was included in the mesa stripe 110 with some components as a result. Many crystal defects are included to the right above field 152 of the selective growth mask 150, this is weak as a crystal, and it is considered to be the cause that it is easier to be divided. That is, in spite of a crystal's carrying out cleavage in the right above field 152 of the selective growth mask 150 and having the **** property with one, it is because cleavage of the near was carried out with the operation gestalt 1. The yield when the same phenomenon is observed not only when cleavage divides a component, but when a scribe divides a component, and a controllability improves this phenomenon in parallel a scribe to the right above field 153 of the selection mask 151 in about 153 right above field of the selection mask 151 compared with a scribe ***** case in the right above field 153 of the selection mask 151 was low.

[0041] Since the component division location by the scribes of all the 4th page at the time of dividing a component can be limited to the right above fields 652 and 653 of the selective growth masks 650 and 651 by this operation morphological child on the other hand, At the time of component division, the scribe happened in the position, the right above field 652 of a selection mask was not included in the mesa stripe 610, and the configuration of a component did not shift from a predetermined configuration (it is the Nogata form, as it observes from the upper part and is shown in drawing 6). Thereby, also in the component shape recognition at the time of mounting a component, the error was able to be reduced and the component mounting yield has also been improved. This point was also a big merit in this operation morphological child.

[0042] (Operation gestalt 4) Next, the operation gestalt of this invention when the barrier layer of the right above field of growth suppression structure remains for the component is explained using the example of light emitting diode. Structural drawing observed from the top face of the light emitting device of this operation gestalt to drawing 7 is shown. The formation approach of a GaN continuation membrane layer and the semi-conductor laminated structure presupposed that it is the same as the

case of the operation gestalt 2 (in explanation of this example of an operation gestalt, the mark of common each class presupposes that it is the same as that of an example 2). Differing from the operation gestalt 2 is the point which the configuration of the mesa 710 containing the In_{0.45}Ga_{0.55}N single quantum well barrier layer 404 has a configuration like drawing 7, and enlarged the size with 390-micrometer angle. For this reason, in the light emitting device of this operation gestalt, it has the form where the In_{0.45}Ga_{0.55}N single quantum well barrier layer 404 located in the right above field 751 of the growth suppression structure slack slot structure 450 at the time of n-GaN continuation membrane layer 401 growth was contained in the mesa 710.

[0043] However, in the light emitting device of this operation gestalt, it has arranged to the central field of a mesa 710 by using p mold electrode 711 as 300-micrometer angle. That is, in the 30-micrometer field, p mold electrode was made not to be formed from the edge of the right above field 751 of the slot structure 450, and the right above field 751. On the other hand, n mold electrode 712 was formed in one corner of a light emitting device where the In_{0.45}Ga_{0.55}N single quantum well barrier layer 404 was removed like drawing 7.

[0044] The p-GaN contact layer 406 consists of p-GaN with comparatively high resistivity, and since the current poured in from p mold contact layer 406 and p mold electrode 711 by considering as such a configuration has 0.4 micrometers and the thin thickness of those, in p mold contact layer 406, a current can hardly diffuse it in a longitudinal direction, but it can pour a current only into the In_{0.45}Ga_{0.55}N single quantum well barrier layer [directly under] 404 of p mold electrode 711.

[0045] As a result of evaluating the property of the light emitting device of the operation gestalt concerned, the chip which has 5% or more of electronic-photon conversion efficiency amounted to 79 of inspected %, and the improvement more marked than the light emitting device constituted by the conventional technique was accepted. Moreover, when the reliability trial (conditions are the same as the operation gestalt 2) of these light emitting devices was performed, the luminescence brightness after 1000-hour progress became 85 - 99% of range to the luminescence brightness of the time of a trial, and it was checked that no light emitting devices are problematic practically.

[0046] As mentioned above, in the light emitting device of an operation gestalt, although the example which produced the light emitting device of a gallium nitride system using the GaN continuation film semi-conductor layer was explained, it cannot be overemphasized that this invention can be applied also when as follows.

(1) When a substrate ingredient and the ingredient of a continuation film semi-conductor layer differ from the ingredient which constitutes a light emitting device (for example, when the case where a substrate is [Si and a continuation film semi-conductor layer] GaAs**s, and a substrate are [continuation membrane layers] GaN(s) in Si and GaAs etc.).

(2) In other than (for example, a ridge stripe, other concavo-convex structures, etc. which were formed on silicon on sapphire) a selective growth mask or slot structure, the structure itself is [the cases (SiNx, SiOx, AlOx, etc.) where the ingredients of the selective growth mask which is growth suppression structure differ, and].

(3) When the sequence of a process is changed so that a substrate may be completely removed before [after forming a continuation film semi-conductor layer] luminous layer formation.

[0047]

[Effect of the Invention] As mentioned above, when a semi-conductor light emitting device was produced on the continuation film semi-conductor layer in which a lattice constant and a coefficient of thermal expansion differ from a substrate by applying this invention, decline in luminous efficiency was prevented and light emitting diode and semiconductor laser with the good yield and high luminous efficiency have been realized. Moreover, this invention enabled it to secure practically sufficient dependability in these light emitting devices.

[Translation done.]

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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view of the semiconductor laser component of the gestalt 1 of operation of this invention.

[Drawing 2] It is the making process Fig. of the semiconductor laser component of the gestalt 1 of operation of this invention.

[Drawing 3] It is drawing showing the median life over the distance from the right above field of a growth mask to a mesa stripe.

[Drawing 4] It is the sectional view of the semi-conductor light emitting device of the gestalt 2 of operation of this invention.

[Drawing 5] It is the making process Fig. of the semi-conductor light emitting device of the gestalt 2 of operation of this invention.

[Drawing 6] It is the sectional view of the semiconductor laser component of the gestalt 3 of operation of this invention.

[Drawing 7] It is the plan of the semi-conductor light emitting device of the gestalt 4 of operation of this invention.

[Drawing 8] It is the making process Fig. of the conventional semi-conductor light emitting device.

[Drawing 9] It is drawing showing the structure of the conventional semi-conductor light emitting device.

[Drawing 10] It is drawing showing the surface density of the crystal transition over the distance from growth suppression structure.

[Description of Notations]

100 Silicon on Sapphire

101 601 GaN buffer layer

102, 602, 401 n-GaN continuation membrane layer

103, 603, 402 n-GaN buffer layer

104 604 n-aluminum0.1Ga0.9N cladding layer

105 605 Multiplex quantum well barrier layer

106, 606, 405 p-aluminum0.1Ga0.9N cladding layer

107 607 406 p-GaN contact layer

110 610 Mesa stripe

111, 611, 408, 711 p mold electrode

112, 612, 407, 712 n mold electrode

150, 151, 650, 651 Selective growth mask

152, 153, 652, 653 Right above field

400 Silicon on Sapphire

403 In0.2Ga0.8N Strain Relaxation Layer

404 In0.45Ga0.55N Single Quantum Well Barrier Layer

410 Mesa

450 Slot Structure

451 751 Right above field

600 SiC Substrate

710 Mesa

[Translation done.]